UNIT VI · LESSON 03

Op-Amps, Timers, PLL, Converters & Power Supplies

ideal op-amp · linear & non-linear circuits · active filters · 555 · PLL · DAC/ADC · rectifiers · regulators · SMPS

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questions in Unit VI
Devices · Amplifiers · Op-amps · Logic

741 IDEAL VS PRACTICAL OP-AMP

Parameter	Ideal	IC 741 (typical)
Open-loop gain A_{OL}	∞	2×10^5 (106 dB)
Input resistance	∞	2 MΩ
Output resistance	0	75 Ω
Bandwidth	∞	1 MHz (unity-gain, GBW)
CMRR	∞	90 dB
Slew rate	∞	**0.5 V/µs**
Input offset voltage	0	1 mV
Input bias current	0	80 nA

- **Virtual short**: $V_+ \approx V_-$ (with negative feedback); no input current
- Slew-rate limit: $\mathbf{f_{max} = SR/(2\pi V_p)}$ → 0.5 V/µs, 10 V peak → **8 kHz**
- Offset compensation: $R_{comp} = R_1 \parallel R_f$ at non-inverting input; null pins 1 & 5 (741)
- Internal blocks: differential amp → gain stage → level shifter → push-pull output
- Frequency compensation (30 pF in 741) → single dominant pole, stable for unity gain

GAIN FORMULAS LINEAR CIRCUITS

Circuit	Output
Inverting	$V_o = -(R_f/R_1)V_i$; $R_{in} = R_1$
Non-inverting	$V_o = (1 + R_f/R_1)V_i$; R_{in} very high
Voltage follower	$V_o = V_i$ (gain 1, buffer)
Summing (inverting)	$V_o = -R_f(V_1/R_1 + V_2/R_2 + \ldots)$
Difference	$V_o = (R_f/R_1)(V_2 - V_1)$ (matched)
Integrator	$V_o = -(1/RC)\int V_i\,dt$
Differentiator	$V_o = -RC\,dV_i/dt$
Instrumentation amp (3 op-amp)	$V_o = (1 + 2R/R_G)(R_3/R_2)(V_2 - V_1)$
I-to-V (transimpedance)	$V_o = -I_{in}R_f$
V-to-I	$I_L = V_i/R_1$
Log amplifier	$V_o \propto -V_T \ln(V_i/(RI_S))$

- Practical integrator: R_f across C (limits low-frequency gain); differentiator: R in series with C

GAIN FORMULAS LINEAR CIRCUITS (CONTD.)

- Square wave into integrator → **triangular**; triangle into differentiator → **square**

RC + OP-AMP ACTIVE FILTERS

- First-order LPF: $f_c = 1/(2\pi RC)$, −20 dB/decade; pass-band gain $1 + R_f/R_1$
- Second-order **Sallen–Key** (VCVS) Butterworth: −40 dB/decade, gain A = **1.586** (Q = 0.707)
- Each order adds 20 dB/decade roll-off
- Band-pass: $f_0 = \sqrt{(f_L f_H)}$; $Q = f_0/BW$ (Q > 10 → narrow band)
- **Notch (band-reject)** filter: twin-T (50 Hz hum)
- **All-pass** filter: phase shift only
- Advantages over passive: gain, no inductors, buffering

PHASE-LOCKED LOOP PLL

- Blocks: **phase detector** → **loop filter (LPF)** → **VCO** (feedback)
- **Lock range** (holds lock) **> capture range** (acquires lock)
- 565 PLL: free-running $f_o = 0.25/(R_T C_T)$
- Applications: FM demodulation, **frequency synthesis** (÷N in feedback → $f_{out} = N f_{ref}$), clock recovery, FSK demodulation, AM detection
- VCO (566): voltage-to-frequency; frequency ∝ control voltage

COMPARATORS NON-LINEAR CIRCUITS

- **Comparator**: open loop; output $\pm V_{sat}$; zero-crossing detector
- **Schmitt trigger** (regenerative comparator): $V_{UT}, V_{LT} = \pm\beta V_{sat}$, $\beta = R_2/(R_1 + R_2)$; hysteresis $V_H = 2\beta V_{sat}$
- **Precision rectifier** (super diode): rectifies mV signals
- **Astable multivibrator**: $T = 2RC \ln((1 + \beta)/(1 - \beta)) \rightarrow T \approx 2.2RC$ for $\beta = 0.5$
- **Monostable**, triangular-wave generator, **sample-and-hold**, clipper, clamper, peak detector

IC NE555 555 TIMER

- Internal: two comparators (thresholds **⅔V_{CC}** and **⅓V_{CC}**), SR flip-flop, discharge transistor, output stage
- **Monostable**: pulse width **T = 1.1 RC**
- **Astable**: $t_H = 0.693(R_A + R_B)C$, $t_L = 0.693R_BC$
- **$f = 1.44/((R_A + 2R_B)C)$**; duty cycle $D = (R_A + R_B)/(R_A + 2R_B)$ (> 50 %)
- Diode across R_B → D ≤ 50 % possible
- Example R_A = 1 kΩ, R_B = 10 kΩ, C = 0.1 µF → f ≈ **686 Hz**, D ≈ 52.4 %
- Pins: 1 GND, 2 trigger, 3 output, 4 reset, 5 control voltage, 6 threshold, 7 discharge, 8 V_{CC}
- Uses: timers, PWM, frequency divider, missing-pulse detector, ramp generator

DIGITAL → ANALOG DAC

- **Resolution** = $V_{FS}/(2^n - 1)$ (step size); n bits → 2^n levels
- **Weighted-resistor DAC**: resistors R, 2R, 4R … $2^{n-1}R$ — wide range, inaccurate for large n
- **R–2R ladder**: only two resistor values → preferred
- $V_o = -V_{ref}(R_f/R)(b_1/2 + b_2/4 + \ldots + b_n/2^n)$ (R–2R type)
- Specs: resolution, accuracy, monotonicity, **settling time**, linearity
- 8-bit, 10 V full scale → step ≈ **39.2 mV** (10/255)

ANALOG → DIGITAL ADC

Type	Conversion time	Feature
Flash (parallel)	fastest (1 clock)	**$2^n - 1$ comparators**
Successive approximation (SAR)	**n clock cycles**	common, medium speed
Counter (ramp)	up to 2^n clocks	simple, slow
Tracking (servo)	follows input	—
Dual-slope integrating	slow	high accuracy, **noise rejection** (DVMs)
Sigma–delta	oversampling	high resolution audio

- Quantisation error ±½ LSB
- 8-bit SAR with 1 MHz clock → **8 µs** conversion
- Flash 8-bit → 255 comparators

AC → DC RECTIFIERS

Parameter	Half-wave	Full-wave (centre-tap)	Bridge
V_{dc}	V_m/π	$2V_m/\pi$	$2V_m/\pi$
I_{rms}	$I_m/2$	$I_m/\sqrt{2}$	$I_m/\sqrt{2}$
Ripple factor	**1.21**	**0.48**	**0.48**
Efficiency	**40.6 %**	**81.2 %**	81.2 %
PIV per diode	V_m	**$2V_m$**	V_m
Ripple frequency	f	2f	2f
TUF	0.287	0.693	0.812
Diodes	1	2	4

AC → DC RECTIFIERS (CONTD.)

- **Ripple factor $\gamma = \sqrt{((I_{rms}/I_{dc})^2 - 1)}$**
- Capacitor filter (full wave): $\gamma = 1/(4\sqrt{3}\, f\, C\, R_L)$; ripple $V_{r(pp)} \approx I_{dc}/(2fC)$
- L filter: $\gamma = R_L/(3\sqrt{2}\,\omega L)$
- LC (choke-input) filter: $\gamma = 1/(6\sqrt{2}\,\omega^2 LC) \approx 1.19/(LC)$ (L in H, C in μF, 50 Hz) — independent of load
- **Voltage multipliers**: doubler, tripler

STABLE DC REGULATORS

- **Line regulation** = $\Delta V_o/\Delta V_{in}$; **load regulation** = $(V_{NL} - V_{FL})/V_{FL} \times 100\ \%$
- **Zener shunt regulator**: $R_s = (V_{in} - V_z)/(I_z + I_L)$; Zener absorbs load changes
- **Series (transistor) regulator**: pass transistor + error amplifier + reference
- **IC regulators**: 78xx (positive: 7805 = +5 V), 79xx (negative), **LM317** adjustable: **$V_o = 1.25(1 + R_2/R_1)$**, 723 general-purpose
- Dropout voltage ≈ 2 V (78xx); LDO regulators ≈ 0.1–0.5 V
- Protection: current limiting, fold-back, thermal shutdown

Q → A RAPID RECALL

Slew rate of 741	0.5 V/μs
Gain of inverting amp, R_f = 100 k, R_1 = 10 k	−10
Op-amp circuit with gain 1, high Z_{in}	voltage follower
Integrator with square-wave input gives	triangular wave
Comparator with hysteresis	Schmitt trigger

SWITCHING SUPPLIES SMPS

- Transistor switched at high frequency (20 kHz – MHz), PWM control → **efficiency 70–95 %**, small magnetics

Converter	Output
Buck	$V_o = D\, V_{in}$ (step-down)
Boost	$V_o = V_{in}/(1 - D)$ (step-up)
Buck–boost	$V_o = -D\, V_{in}/(1 - D)$ (inverted)
Flyback / forward	isolated (transformer)

- Linear regulator: simple, low noise, poor efficiency (V_o/V_{in}); SMPS: efficient, EMI/ripple

Q → A RAPID RECALL (CONTD.)

555 monostable pulse width	1.1 RC
555 thresholds	⅓ and ⅔ V_{CC}
PLL range that is larger	lock range
Fastest ADC	flash
Comparators in 4-bit flash ADC	15

Q → A RAPID RECALL (CONTD.)

Ripple factor of full-wave rectifier	0.48
PIV in centre-tap rectifier	$2V_m$
Output of LM317 with $R_2/R_1 = 3$	5 V
Buck converter output, D = 0.4, 12 V in	4.8 V

TRAP EXAM TRAPS

- Virtual ground holds only with negative feedback
- Ripple frequency of a full-wave rectifier is **2f** (100 Hz on 50 Hz mains)
- Bridge diodes see PIV = V_m, centre-tap diodes see $2V_m$
- Dual-slope ADC is slow but very accurate (rejects mains hum)
- 555 astable duty cycle cannot go below 50 % without a diode