UNIT VIII · LESSON 01

8085 Microprocessor

architecture · registers & flags · pins · addressing modes · instruction set · timing · interrupts · stack · programs

20 questions in Unit VIII

8085 · 8086 · 8051 · ARM · RTOS

FEATURES 8085 AT A GLANCE

- Intel, **1976**, 8-bit, **NMOS**, single **+5 V** supply, 40-pin DIP
- **8-bit data bus**, **16-bit address bus → 64 KB** memory; 256 I/O ports (8-bit port address)
- Clock: crystal frequency/2 → 3 MHz (8085A), 5 MHz (8085AH-2)
- **Multiplexed** lower address/data bus **AD_0–AD_7** (demultiplexed with **ALE** + latch 74LS373)
- 74 instructions (246 opcodes), 5 hardware interrupts, serial I/O (SID, SOD)

5 FLAGS FLAGS

Flag	Set when
S (D7)	result MSB = 1 (negative)
Z (D6)	result = 0
AC (D4)	carry from bit 3 to bit 4 (BCD, used by DAA)
P (D2)	result has **even** number of 1s
CY (D0)	carry/borrow out of MSB

- Example: A = 9AH + 7BH = **15H**, CY = 1, Z = 0, S = 0, P = 0 (15H = 0001 0101 → three 1s), AC = 1
- INR/DCR affect all flags **except CY**; logical AND sets AC = 1 (8085), OR/XOR reset CY and AC

PROGRAMMER'S MODEL REGISTERS

Register	Size	Use
A (accumulator)	8	ALU operand & result
B, C, D, E, H, L	8 each	general purpose; pairs **BC, DE, HL** (16-bit)
HL	16	memory pointer (M = [HL])
SP	16	stack pointer
PC	16	address of next instruction
Flag register	8 (5 used)	S Z – AC – P – CY
Temporary, instruction register	8	not accessible to programmer

- **PSW** = A + flags (used in PUSH PSW / POP PSW)

40 PINS PIN GROUPS

- Address: **A_8–A_{15}** (high), AD_0–AD_7
- Control & status: **ALE**, RD', WR', **IO/M'**, S_0, S_1
- IO/M' S_1 S_0: opcode fetch **011** (IO/M' = 0, S1 = 1, S0 = 1), memory read 010, memory write 001, I/O read 110, I/O write 101, halt (Z) 00
- Interrupts: **TRAP**, RST 7.5, RST 6.5, RST 5.5, **INTR**, INTA'

40 PINS PIN GROUPS (CONTD.)

- DMA: **HOLD**, **HLDA**; **READY** (slow peripherals → wait states)
- RESET IN', RESET OUT, X1, X2, CLK OUT, SID, SOD, V_{CC}, V_{SS}

SET INSTRUCTION GROUPS

Group	Instructions
Data transfer	MOV, MVI, LDA, STA, LDAX, STAX, LXI, LHLD, SHLD, XCHG, IN, OUT
Arithmetic	ADD, ADC, ADI, SUB, SBB, SUI, INR, DCR, INX, DCX, **DAD**, **DAA**
Logical	ANA, ANI, ORA, ORI, XRA, XRI, CMP, CPI, CMA, CMC, STC, RLC, RRC, RAL, RAR
Branch	JMP, JC/JNC, JZ/JNZ, JP/JM, JPE/JPO, CALL (conditional), RET, RST n, PCHL
Stack, I/O & machine control	PUSH, POP, XTHL, SPHL, EI, DI, RIM, SIM, HLT, NOP

- **Instruction sizes**: 1-byte (MOV A,B), 2-byte (MVI A,32H; IN 01H), 3-byte (LXI H,2050H; JMP; LDA)
- `XRA A` clears A and CY; `CMP B`: A < B → CY = 1, A = B → Z = 1
- `DAD B`: HL ← HL + BC (only CY affected); `INX` / `DCX` affect **no flags**
- `RLC` rotate left (D7 → CY and D0); `RAL` through carry

5 MODES ADDRESSING MODES

Mode	Example	Meaning
Immediate	`MVI A, 32H`	data in instruction
Register	`MOV A, B`	data in register
Direct	`LDA 2050H`	16-bit address in instruction
Register indirect	`MOV A, M` / `LDAX B`	address in register pair
Implied (implicit)	`CMA`, `RAL`	operand implied (A)

LIFO STACK & SUBROUTINES

- Stack grows **downward** (SP decrements by 2 on PUSH/CALL)
- `PUSH B`: SP−1 ← B, SP−2 ← C, SP ← SP − 2
- CALL saves the return address (PC) on the stack; RET pops it
- `LXI SP, 2FFFH` initialises the stack (top of RAM)

T-STATES TIMING

- **Machine cycles**: opcode fetch (**4 T** or 6 T), memory read (3 T), memory write (3 T), I/O read/write (3 T), interrupt acknowledge

Instruction	Bytes	Machine cycles	T-states
MOV A, B	1	1 (OF)	4
MVI A, data	2	2 (OF, MR)	7
LDA addr	3	4 (OF, MR, MR, MR)	13
STA addr	3	4	13
LXI H, data	3	3	10
MOV A, M	1	2	7
CALL addr	3	5	18
RET	1	3	10
PUSH B	1	3	12
JNZ (taken / not)	3	3 / 2	10 / 7

- Time = T-states × clock period (3 MHz → 0.333 µs)
- Delay loop: count = (delay − overhead)/(T per loop × T_{clk})

PRIORITY INTERRUPTS

Interrupt	Type	Vector	Priority
TRAP	**non-maskable**, edge + level	0024H	1 (highest)
RST 7.5	maskable, **edge** (rising)	003CH	2
RST 6.5	maskable, level	0034H	3
RST 5.5	maskable, level	002CH	4
INTR	maskable, **non-vectored**	via RST n from device	5 (lowest)

- Software RST n vector = **n × 8** (RST 7 → 0038H)
- **SIM** sets masks & serial output; **RIM** reads masks, pending interrupts, serial input
- EI/DI enable/disable all maskable interrupts

ASSEMBLY SAMPLE PROGRAMS

```
; add two 8-bit numbers at 2050H, 2051H
LDA 2050H      ; A <- [2050]
MOV B, A
LDA 2051H
ADD B          ; A <- A + B
STA 2052H      ; store sum
HLT
```

```
; count down delay loop (10 x)
      MVI C, 0AH
LOOP: DCR C          ; 4 T
      JNZ LOOP       ; 10 T (7 T last)
      HLT
```

- Loop T-states = 7 (MVI) + 10 × 4 + 9 × 10 + 7 = **144 T**

SUPPORT PERIPHERAL CHIPS

IC	Function
8155 / 8156	RAM + I/O ports + timer
8255 PPI	programmable peripheral interface: 3 ports (A, B, C), modes 0, 1, 2
8253 / 8254	programmable interval timer: 3 × 16-bit counters, 6 modes
8259 PIC	programmable interrupt controller: 8 levels, cascadable to 64
8257 / 8237	DMA controller (4 channels)
8251 USART	serial communication
8279	keyboard / display controller

- 8255 BSR mode sets/resets individual port C bits

Q → A RAPID RECALL

8085 address bus width	16 bits (64 KB)
Signal to demultiplex AD_0–AD_7	ALE
Flag not affected by INR	CY
Parity flag set for	even number of 1s
Highest-priority interrupt	TRAP
Non-vectored interrupt	INTR
Vector of RST 6.5	0034H
T-states of opcode fetch	4
Bytes in LXI H, 2500H	3
Instruction that adds register pair to HL	DAD

Q → A RAPID RECALL (CONTD.)

Instruction to read interrupt masks	RIM
Programmable interval timer IC	8253 / 8254

TRAP EXAM TRAPS

- INX/DCX change no flags — a loop using `DCX` then `JNZ` needs an explicit test
- TRAP is non-maskable; RST 7.5 is edge-triggered (latched)
- 8085 has 16-bit address but 8-bit I/O port address
- `CMP` changes only flags, not A
- `SUB A` clears A and sets Z = 1